METHOD OF FORMING A TRANSISTOR HAVING MULTIPLE CHANNELS AND STRUCTURE THEREOF

Related Application

5

This application is related to United States patent application serial number 10/074,732, entitled "Method of Forming A Vertical Double Gate Semiconductor Device And Structure Thereof" filed February 13, 2002, and assigned to the assignee hereof.

10

Field of the Invention

This invention relates generally to semiconductors, and more specifically, to the manufacture of and the structure of semiconductor devices.

15

Background of the Invention

As semiconductor devices continue to become smaller in size, the devices must be what is known in the industry as "scalable". That is, the
20   devices must continue to be able to be made with reduced dimensions and still function at the required specifications. Traditionally, MOSFETs have been implemented with a single control electrode or gate on a planar substrate. The gate is placed between a source and drain electrode and functioned to create a channel for controlling the amount of current conducted by the MOSFET.
25   Because there is a gate electrode to control the channel only on one side of the channel, there is only a single source of control of the channel. Single control

of the channel leads to undesired leakage current (i.e. electron or hole flow) between the source and drain when the transistor is intended to be non-conductive.

An improved structure that was proposed was the use of a two-gate transistor with the gates on both sides of a thin silicon channel. This arrangement increases the electrostatic coupling between the gates and the channel relative to the single gate device. As a result, the drive current of the transistor is increased and the leakage current is decreased. One type of transistor having two gates is known in the art as double gate or dual gate FinFETs, in which the channel consists of a single pillar or slab (a fin) that is oriented perpendicular to the plane of a substrate for a given area overlying the substrate. Additional channel width for a transistor requires additional circuit area to provide the additional channel width. For example, known planar MOSFETs and FINFETs having multiple channels are formed laterally and thus require significant additional area.

The effective channel width of a FinFET transistor is only on the surface of a single silicon fin. The dimensions of the fin determine the characteristics of the device. It is desirable that the fin be thinner than the gate length in order to get good short channel control. However, lithographically or spacer defined dimensions do not offer as much manufacturing control as grown layers to form a transistor channel.

Brief Description of the Drawings

The present invention is illustrated by way of example and is not limited by the accompanying figures, in which like references indicate similar

5   elements.

FIG. 1 illustrates in cross-sectional form initial layers of a semiconductor device in accordance with the present invention;

FIG. 2 illustrates in cross-sectional form further processing of the semiconductor device of FIG. 1;

10   FIG. 3 illustrates in cross-sectional form a top view of the semiconductor device of FIG.2;

FIG. 4 illustrates in cross-sectional form patterning of the semiconductor device of FIG. 2;

FIG. 5 illustrates in cross-sectional form a first form of processing of the

15   semiconductor device of FIG. 4;

FIGs. 6 and 7 illustrate in cross-sectional form an alternate form of processing of the semiconductor device of FIG. 4;

FIG. 8 illustrates in cross-sectional form continuation of the processing of the semiconductor device of FIG. 5;

20   FIG. 9 illustrates in cross-sectional form continuation of the processing of the semiconductor device of FIG. 8 including the formation of multiple overlying channels;

FIG. 10 illustrates in perspective form the semiconductor device illustrated in FIG. 9;

25   FIG. 11 illustrates in cross-sectional form removal of a portion of layers of the semiconductor device of FIG. 9; and

FIG. 12 illustrates in cross-sectional form completion of the semiconductor device.

Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For

5   example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve the understanding of the embodiments of the present invention.

Detailed Description

10

Illustrated in FIG. 1 is a semiconductor device 10 having a substrate 12. In one form the semiconductor device 10 is an FET (field effect transistor). The substrate 12 may be formed of any type of material, either conductive, semi-conductive or insulative. In one form, substrate 12 is single crystal silicon.

15   Other forms of substrate 12 may include silicon, silicon on insulator, silicon on sapphire, and silicon on nitride. An insulating layer 14 overlies the substrate 12. Insulating layer 14, in one form, is silicon dioxide. Overlying the insulating layer 14 is a semiconductor layer 16. In one form, semiconductor layer 16 is silicon or silicon germanium, but other semiconductor materials may

20   be used. For example, germanium, silicon germanium carbon, gallium arsenide, gallium nitride and indium phosphide are other appropriate material compositions.

In another form, the integrated circuit substrate 12 is a silicon-on-insulator (SOI) bonded wafer having a silicon layer which functions as

25   semiconductor layer 16. Overlying semiconductor layer 16 is a semiconductor layer 18. While semiconductor layer 18 may be formed of any semiconductor

material, one implementation of semiconductor layer 18 is silicon germanium. In addition, semiconductor layer 18 should be of the same crystallinity as the material used for semiconductor layer 16 but having differing etch properties (i.e. different etch rates). A plurality of additional overlying semiconductor

5   layers is formed overlying semiconductor layer 18. In the illustrated form, semiconductor layer 20, semiconductor layer 22 and semiconductor layer 24 are formed. While various materials may be implemented, semiconductor layers 16, 20 and 24 should be formed of the same material in order to have a same first etch rate. Similarly, semiconductor layers

10   18 and 22 should be formed of the same material in order to have a same second etch rate. Typically, substrate 12, insulating layer 14 and semiconductor layer 16 are formed as an SOI starting material. The creation thereof may be vary. For example, insulating layer 14 may be thermally grown or deposited onto substrate 12 and bonded with semiconductor layer 16. In one

15   form, semiconductor layers 18, 20, 22 and 24 are formed by epitaxial growth. In other forms, semiconductor layers 18, 20, 22 and 24 may be formed using atomic layer deposition or molecular beam epitaxy. The compositions of silicon and silicon germanium and thicknesses thereof are controlled by the ambient gas flow, temperature and time in a conventional manner such as

20   epitaxial growth. Typical thickness for these layers varies between two hundred to four hundred Angstroms. The illustrated thickness is not necessarily drawn to scale.

Illustrated in FIG. 2 is further processing of semiconductor device 10 wherein a patterned layer 26 is formed over a predetermined portion of

25   semiconductor layer 24. In one form, the patterned layer 26 is nitride. However, other materials that function as a protective barrier material may be

used. Examples of other materials suitable for use as the patterned layer 26 include, by way of example only, photoresist, oxide, and an organic anti-reflective coating (ARC).

Illustrated in FIG. 3 is a top view of the semiconductor device 10 formed as in FIG. 2. From the top, patterned layer 26 has two end portions that are much wider than a connecting portion. The connecting portion forms a channel region and the two ends respectively form a source and a drain that respectively function as first and second current handling terminals, current handling electrodes or current electrodes. The source and drain are not doped (i.e. implanted) until later steps after formation of the gate of the semiconductor device. The width of the channel region is designated as "w". Patterned layer 26 is formed over semiconductor layer 24. Patterned layer 26 functions as a protective barrier to permit selective etching of the underlying semiconductor layers. To further correlate FIG. 3 with FIG. 2, a cross-sectional line in FIG. 3 illustrates the FIG. 2 view.

Illustrated in FIG. 4 is further processing of semiconductor device 10. As illustrated, the semiconductor layers 16, 18, 20, 22 and 24 are etched or removed from those areas not protected by the patterned layer 26. The resulting structure exposes insulating layer 14 and leaves a stack of semiconductor layers in which alternating layers are, in one form, a same material with a same etch rate property. Instead of using a same material in alternating layers, the alternating layers have a different etch rate. Semiconductor layers 16, 20 and 24 have etch rates that differ from semiconductor layers 18 and 22. Another way of stating this property is to consider the layers beginning with semiconductor layers 16 and 18 as being odd and even layers, alternately, and so on as additional semiconductor layers are added. Semiconductor layers in

odd numbered layers need only to have a different etch rate property than the layers in even numbered layers.

Illustrated in FIG. 5 is further processing of semiconductor device 10 wherein an isotropic etch is performed by placing all of the semiconductor
5   device 10 in an etchant that is selective to etching semiconductor layers 18 and 22. In one form, the etchant is a mixture of nitric acid, hydrogen peroxide and hydrofluoric acid. It should be understood that in another form the etching could be implemented by using an etchant that is selective to semiconductor layers 16, 20 and 24. Referring back to FIG. 3, the varying widths of patterned
10 layer 26 directly influences how the FIG. 5 semiconductor device 10 looks. All exposed surfaces of semiconductor layers 18 and 22 are etched to some extent. The central region of patterned layer 26 has a width, w, that is significantly smaller than the end regions thereof. The smaller width central region allows the complete removal of semiconducting material in a central region of each of
15 semiconductor layers 18 and 22 to respectively form cavities 30 and 32, respectively. Additional to cavities 30 and 32, the remaining exposed portions of semiconductor layers 18 and 22 are also etched. At the edges, complete removal of the semiconductor layers 18 and 22 forms notches 34, 36, 38 and 39. Because the etch that is performed created cavities 30 and 32, it is certain that
20 the amount of inward isotropic etching that occurs at the edges of semiconductor layers 18 and 22 is a length of at least w or greater.

Illustrated in FIG. 6 is an alternative embodiment of the patterned etch of semiconductor layers 18 and 22. In this form, an extra processing step is required by the presence of notches 34, 36, 38 and 39 is avoided. A protective
25 layer 28 is patterned overlying semiconductor device 10. In particular, only a portion of the stack of semiconductor layers is allowed to be exposed. This

exposed area will form the channel region of the semiconductor device 10. In one form the protective layer 28 is implemented with silicon dioxide or a photoresist. Other materials may be used such as a nitride.

Illustrated in FIG. 7 is a later step in the alternative embodiment begun in
5   FIG. 6. An isotropic is performed by placing all of the semiconductor device 10 in an etchant that is selective to etching semiconductor layers 18 and 22. It should be understood that in another form the etching could be implemented by using an etchant that is selective to semiconductor layers 16, 20 and 24. All exposed surfaces of semiconductor layers 18 and 22 are etched to some extent.
10   The sides of semiconductor layers 18 and 22 directly underneath the opening in protective layer 28 are exposed and etched all the way through to respectively form cavities 40 and 42, respectively. Because the etch goes completely through the width, w, of the central portion of patterned layer 26, the amount of inward isotropic etching that occurs at the edges of cavities 40 and 42 into
15   semiconductor layers 18 and 22, respectively, is a lateral amount of at least one-half of w (w/2) or greater since the etching of cavities 40 and 42 is occurring from two sides. It should however be apparent that due to effects such as loading, non-uniform etch rates between the central region and the edge regions are possible thereby resulting in the edge etch dimension being slightly less
20   than (w/2). To conclude the selective etching of semiconductor layers 18 and 22, the protective layer 28 is removed.

Assume that the first form of the etching of semiconductor layers 18 and 22 is implemented for discussion of further processing. Illustrated in FIG. 8 is the resulting structure from FIG. 5. In FIG. 8, a thin dielectric or insulating
25   layer is formed on all exposed surfaces of the semiconductor layers 16, 18, 20 22 and 24. In particular, thin oxide layers 50 and 52 are formed on the surfaces

of cavities 40 and 42, respectively. Thin oxide layer 50 is formed on the left edges of semiconductor layers 16, 18, 20, 22 and 24 and thin oxide layer 56 is formed on the right edges of semiconductor layers 16, 18, 20, 22 and 24. It should be understood that when viewed in perspective form, the thin oxide

5   layers 50, 52, 54 and 56 are a continuous single oxide layer. There will be minimal variation in the thickness of the oxide layer over semiconductor layers of differing materials. The thin oxide layer within the cavities 40 and 42 functions as a gate dielectric. The thin oxide layer will also function as an etch stop layer in a subsequent processing step described below. In one form, the

10   oxide layer is thermally grown and is silicon dioxide. Other forms of the thin oxide layer may be dielectrics that are deposited, such as oxides, metal oxides or oxy-nitrides.

Illustrated in FIG. 9 is further processing of semiconductor device 10 wherein a gate electrode 60 and a masking (i.e. blocking) layer 80 are deposited

15   and patterned to form the illustrated gate. A gate is formed in multiple portions in different vertical layers as noted by the cross-hatching in FIG. 9. The multiple layers of the gate surround the channel regions 72, 74 and 76 and form a vertical stack with respect to a horizontal reference coplanar with a top surface of the substrate 12. In other words, the channel regions 72, 74 and 76

20   are physically separated at least by portions of a control terminal material used to form gate electrode 60. In one form, gate electrode 60 is either a metal or polysilicon, either in doped or undoped form. Due to the conformal nature of the deposition of polysilicon, the gate electrode forms in each of cavities 40 and 42 and is removed (i.e. etched) conformal to the desired pattern location and

25   etch rate. The etch results in former cavity 40 having an edge cavity 78 and an edge cavity 79. Similarly, former cavity 42 has an edge cavity 81 and an edge

cavity 83. These edge cavities are desired and function as spacers isolating the source and drain regions from the gate and will be filled with insulating spacer material to be described below. To the left of the gate electrode 60 is a source or drain region designated as "S/D" and to the right of the gate electrode 60 is a

5 drain or source region designated as "D/S" that function as current handling terminals. Each current handling terminal has a width that is substantially equal to a first value. Each of the channel regions 72, 74 and 76 has a width that is substantially equal to a second value wherein the first value is greater than the second value. At this point in the processing, these source and drain regions are

10 doped with an ion implantation. An N type implant is performed for an NMOS transistor and a P type implant is performed for a PMOS transistor. Masking layer 80 and gate electrode 60 function as blocking layers to prevent the implant from entering the channel regions. It should be noted that a transistor has been formed having multiple channels that are compact and vertically aligned in

15 overlying fashion. The channel dimensions between the various portions of gate electrode 60 may be formed with extremely fine precision because the channels are grown in the vertical direction. This is a very important feature. In multiple gate transistors, the ability to control the dimensions of the transistor channel control other electrical parameters such as leakage current and short

20 channel effects.

At this point, an integrated circuit having a transistor with source, drain and gate electrodes has been formed. The transistor has multiple overlying channel regions formed under or between multiple gate layers. The gate layers are a common material and are represented by the cross-hatched regions, such

25 as the region of gate electrode 60. The gate electrode 60 functions as a control terminal and is shaped to fully loop around channel regions 72, 74 and 76.

Alternating layers of the semiconductor layers, such as semiconductor layers 16, 20 and 24 contain a channel region connected to the source and drain on either end. The source and drain have a different conductivity than the channel as a result of source/drain implants. It should be noted that the source/drain that

5 is formed by the ion implantation of semiconductor layers 16, 18, 20, 22 and 24 is formed of a substantially homogenous crystal lattice to have homogenous crystallinity. Similarly, the plurality of channels formed by channel regions 72, 74 and 76 is also formed of a substantially homogenous crystal lattice to have homogenous crystallinity.

10 Illustrated in FIG. 10 is a perspective view of the semiconductor device 10 of FIG. 9. For convenience of illustration, the same elements are numbered identically. Again, it should be noted that the shape of the source and drain columns may vary. Although the original shape may begin as a straight-edge structure, the various etching steps tend to round or smooth the source and drain

15 regions resulting in the circular forms. All of the semiconductor layers 18, 20, 22 and 24 are grown from the same seed layer, semiconductor layer 16. This provides substantially monocrystalline channels. Monocrystalline silicon provides better transistor characteristics (e.g. mobility, dopant activation and oxide quality) than polycrystalline or amorphous silicon. Any number of

20 semiconductor layers may be implemented. Additional semiconductor layers create further channel surface area and thus increased transistor drive capability. This additional drive capability is provided without increasing lateral transistor area and is therefore a very compact and size efficient transistor. While the cross-sectional views of the previous illustrations do not lend themselves to

25 show how the gate electrode 60 loops around channel region 74 and channel region 76, it is clear from the perspective view of FIG. 10 that the gate electrode

goes through former cavities 40 and 42 to form a loop around channel region 74 and channel region 76. Channel region 72, the lowest or bottom-most channel region has only overlying gate electrode material. It should be noted that the transistor embodied by semiconductor device 10 may be implemented with a

5   plurality of channels, such as channel 16 and channel 20, that vary in thickness and have different thickness rather than a uniform thickness. Since the structure is a stack structure, the various layers can readily be formed with differing thickness. Further, the separation distance between any two of the plurality of channels may be different. In other words, semiconductor layer 18 may be

10   implemented with a thickness that is different than the thickness of semiconductor layer 22. In this form, at least two of the plurality of channels are separated from an adjacent channel by a different amount. The variability in thickness provides flexibility in adjusting the desired transistor characteristics. Additionally, it should be understood that in the FIG. 10

15   perspective, the gate electrode 60 extends symmetrically from the other side of the transistor that is not visible from the view. In other words, gate electrode 60 is symmetric and extends away from the channel region a predetermined desired amount.

Illustrated in FIG. 11 is a cross-sectional view of semiconductor device

20   after yet further processing from the structure of FIG. 9. A spacer 84 is formed which isolates the gate from the source and drain. At this point part or all of semiconductor layers 18 and 22 are removed by an isotropic etch. If semiconductor layers 18 and 22 are formed of silicon germanium, it may be desirable to remove these layers and re-grow silicon in its place. This step is

25   application specific. In some applications it is desired to remove silicon germanium because the composition may result in a germanicide and silicides

on silicon have lower resistivity than germanicides. In other applications, dopant activation properties of germanium may be desirable and therefore the presence of silicon germanium is desired. This etch also removes the thin oxide layers 52 and 56. The semiconductor layers 20 and 24 are suspended at the

5   sides but anchored by the gate and channel structure.

Illustrated in FIG. 12 is a cross-sectional view of semiconductor device 10 wherein additional semiconductor region 96 is selectively grown, usually epitaxially, on all exposed silicon or silicon germanium regions. Semiconductor region 96 functions to reduce the resistance of the source and

10   drain regions of the transistor formed by semiconductor device 10. Semiconductor region 96 also functions as a continuous contact region to the source and drain of the structure. It should be understood that further conventional processing may be implemented such as additional source/drain implanting, thermal activation, salicidation of the source, drain and gate regions

15   and contact structure formation and metal interconnect.

By now it should be appreciated that there has been provided a field effect transistor in an integrated circuit and method of formation that has multiple channel regions that are overlying in an efficient vertical stack structure. The transistor has multiple layers of silicon and gate electrodes and

20   gate dielectric in the channel region. Channel region is increased for a given layout area as compared with conventional multiple channel or multiple fin transistor structures. The increased channel area increases the current drive of the transistor and the control of the channel dimensions contribute to better short channel performance and manufacturability of the transistor. In one form,

25   an integrated circuit has a substrate and an overlying transistor. The structures taught herein provide an efficient method to control the channel dimensions.

Further the separation distance between portions of a same channel may vary and the separation distance between channels of differing transistors may be different or the same depending upon the specific desired application. The transistor has a first channel overlying the substrate, a first portion of a control

5   or gate electrode overlying the first channel, a second channel overlying the first portion of the gate electrode and a second portion of the gate electrode overlying the second channel and connected to the first portion of the gate electrode. A first current handling electrode is connected to the first channel and the second channel. A second current handling electrode is connected to

10   the first channel and the second channel. The method of fabricating a vertical multiple-channel FET device provides an integrated circuit substrate. At least two layers having a first composition with a first etch property overlie the substrate. At least one layer of a second composition having a second etch property also overlie the substrate and alternate with the at least two layers of

15   the first composition. The at least two layers of the first composition and the at least one layer of the second composition are formed to have a substantially homogenous crystallinity. A blocking layer is formed over the at least two layers of the first composition and the at least one layer of the second composition. The blocking layer is patterned to define placement of a first

20   current electrode region, a second current electrode region and a plurality of channels. Exposed portions of the at least two layers of the first composition and the at least one layer of the second composition are etched to form the first current electrode region, the second current electrode region and channel regions extending from the integrated circuit substrate. The at least one layer of

25   the second composition is further etched to remove said at least one layer of the second composition and to form the plurality of channels of the first

composition and located above and below any removed portion of the at least one layer of the second composition. A control electrode dielectric is deposited around each of the plurality of channels. Control electrode material is deposited around the control electrode dielectric. The control electrode material is

5   selectively masked and etched to form a control electrode on top, bottom and sidewall surfaces of at least one of the plurality of channels. A spacer is formed to isolate the control electrode material from the first current electrode region and the second current electrode region.

Although the method and structure taught herein has been disclosed with

10   respect to certain specific steps and materials, it should be readily apparent that various alternatives may be used. Source and drain electrodes may be used with polysilicon material instead of substantially monocrystaline silicon. Gate dielectrics other than silicon dioxide may be used. The height of the gate structure, including specific component elements, may be varied significantly.

15   The gate length may be varied depending upon the specific channel length desired for an application. The gate material may be polysilicon that is insitu doped or implanted, polysilicon germanium or metals such as titanium nitride, tantalum silicon nitride or silicides such as nickel or cobalt silicides or combinations therein. Although the width of the source and drain is illustrated

20   to be greater than the width of each of the channels, the widths could be substantially the same.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any

25   benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all

the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed

5   or inherent to such process, method, article, or apparatus.